

Integrator for measuring magnetic fields

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A voltage integrator designed for interface to a computer is described. It is used to integrate the EMF developed around a loop of wire when the magnetic field through the loop is changed. The integrator is inexpensive, stable, and provides field measurements accurate to 0.1%.

PACS numbers: 07.55. + x

Integrators were built to map magnetic field strength at many points in a large iron electromagnet. Since the magnet has no air gap (the field is used to deflect muons as they pass through the iron), other measurement techniques could not be used. Instead, five by six in. loops of wire were built into the magnet, perpendicular to the field. As the field is changed, the time integral of the EMF developed around each loop is measured. The field change (ΔB) can then be calculated (in Gaussian units) from

$$\int \text{EMF } dt = \frac{1}{c} A \cdot \Delta B,$$

where A is the projected area of the loop perpendicular to the magnetic field.

Since only the change in field is measured, one must know the field strength at some current in order to determine it at others. The existence of a residual field at zero current can make this difficult. The magnet could be degaussed, to establish zero field at zero current. In our application only the field strength at saturation was needed. This is simply half the field change from saturation in one polarity to saturation in the other.

Each integrator circuit produces output pulses which are counted by digital circuitry and analyzed by computer. With no input voltage, the integrators produce about 5000 pulses per second. Positive input voltages reduce this rate and negative voltages increase it.

In operation, the magnetic field is held constant so the computer can measure the zero-input rate. Then the field is reversed and the number of pulses during the reversal is recorded. Finally, the zero-input rate is measured again. The average of the two zero-input rates is used to calculate the expected number of pulses for the duration of the period when the field was changing. Subtracting the expected number from the actual number yields the number of extra pulses due to the field change. Each extra pulse corresponds to a 20.0-G change in magnetic field (for a 30-sq. in. loop).

This method gives results repeatable to 20–30 G when the integration period is 20 seconds. This is about 0.1% of the total field change. In an air gap magnet the above method gave results agreeing with NMR measurements to better than 0.2%. To achieve this accuracy it is necessary to calibrate the integrator by applying a known input voltage. The area (A) of the loop must be known accurately.

The circuit is shown in Fig. 1, where $R1$, $R2$, $C2$, and the op amp (741) form a conventional analog voltage integrator. Whenever the output voltage (V_A) of the analog integrator rises above a critical voltage (V_C), the comparator's (72810) output goes low. At the leading edge of the next clock cycle, this low level appears on the Q output of the flip flop (7474). This turns on transistors $Q1$ and $Q2$, so for the 90 μ s duration of the clock pulse, a current flows through $R3$. This eventually causes V_A

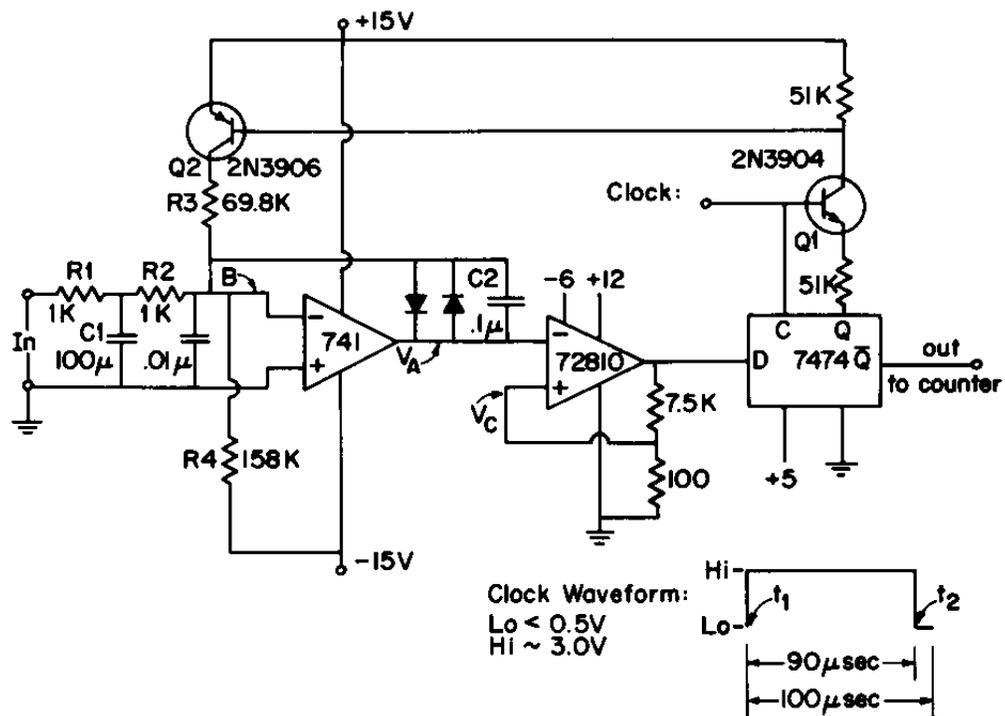


FIG. 1. Schematic diagram of one integrator channel. The circuit produces TTL level pulses at a rate determined by the input voltage.

to drop below V_C , so that at the leading edge of the next clock cycle Q_1 and Q_2 will be turned off. The comparator, by its control over whether V_A is increasing or decreasing, keeps V_A within 0.2 V of V_C .

Since V_A is almost constant, almost no net charge arrives at point B through C_2 . Charge from the input (through R_1 and R_2) is therefore equal to charge departing through R_4 minus that arriving through R_3 . The latter two quantities are known: Charge departs through R_4 at a constant rate and charge through R_3 is proportional to the number of output pulses.

With the values of R_1 and R_2 shown, the circuit saturates at input voltages beyond ± 200 mV. Capacitor C_1 filters out high frequency/small amplitude changes in magnetic field caused by power supply ripple. Resistors R_1 – R_4 are metal film for stability. For the ± 15 V supplies I found 7815 and 7915 regulator chips to be sufficiently stable. There should be $0.01 \mu\text{F}$ shunt capacitors from the +12, +5, and -6 V pins of the ICs to ground. The input grounds should be connected to the power grounds at only one point in a system of integrators, to avoid ground loops.

Many channels of this circuit can be driven by the same clock. All the outputs assume a high or low state at the same moment (t_1) and hold that state for $100 \mu\text{s}$. This makes multiplexing convenient. In our application, during the $100 \mu\text{s}$, 72 binary words (one for each integrator) were sequentially read out of RAM chips, incremented if the corresponding integrator output was high, and then written back into RAM. For a smaller number of integrators it might be more convenient to run each into its own counter. If so, the outputs should be ANDed with the clock pulse to separate contiguous output pulses.

The suggestions of Richard Sumner were of great help to this project. This work was supported by the National Science Foundation.

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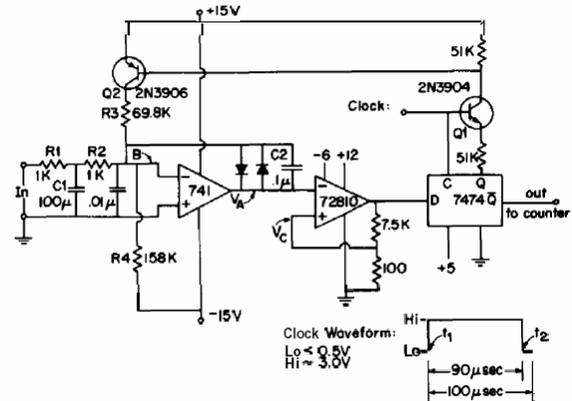


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Many channels of this circuit can be driven by the same clock. All the outputs assume a high or low state at the same moment (t_1) and hold that state for 100uS . This makes multiplexing convenient. In our application, during the 100us , 72 binary words (one for each integrator) were sequentially read out of RAM chips, incremented if the corresponding integrator output was high, and then written back into RAM. For a smaller number of integrators it might be more convenient to run each into its own counter. If so, the outputs should be ANDed with the clock pulse to separate contiguous output pulses.

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