Future Technology Devices International Ltd

UM245R USB - Parallel FIFO Development Module

Datasheet

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1 Introduction

The UM245R is a development module which uses FTDI's FT245RL, the latest device to be added to FTDI's range of USB to parallel FIFO interface Integrated Circuit Devices. The FT245R is a USB to parallel FIFO interface, with the new FTDIChip-ID™ security dongle feature. In addition, asynchronous and synchronous bit bang interface modes are available. USB to parallel designs using the FT245R have been further simplified by fully integrating the external EEPROM, clock circuit and USB resistors onto the device. The FT245R adds a new function compared with its predecessors, effectively making it a "2-in-1" chip for some application areas. A unique number (the FTDIChip-ID™) is burnt into the device during manufacture and is readable over USB, thus forming the basis of a security dongle which can be used to protect customer application software from being copied. The UM245R is supplied on a PCB which is designed to plug into a standard 15.0mm (0.6") wide 24 pin DIP socket. All components used, including the FT245RL are Pb-free (RoHS compliant).

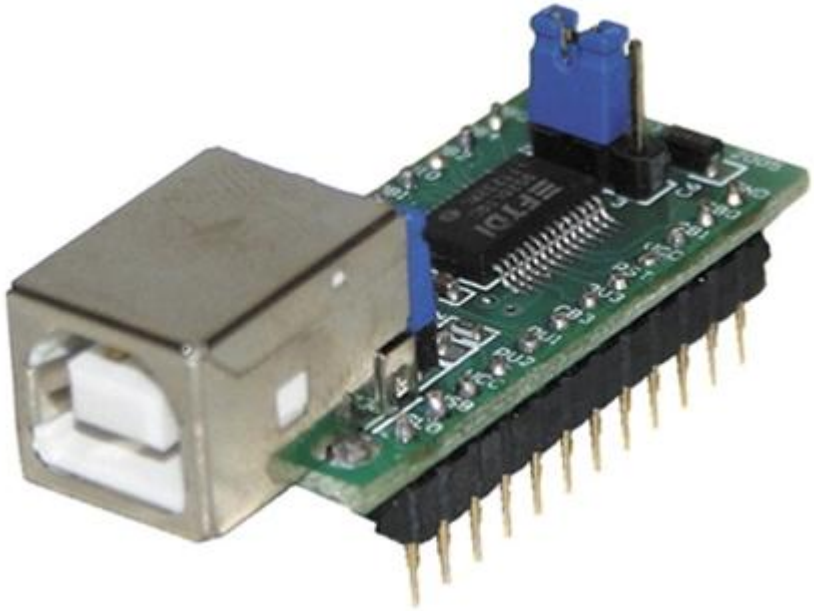

Figure 1.1 – UM245R USB to Parallel FIFO Development Module

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2 Typical Applications

- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software / Hardware Encryption Dongles

2.1 Driver Support

Royalty-Free VIRTUAL COM PORT (VCP) DRIVERS for:

- Windows 7 32,64-bit
- Windows Vista
- Windows XP 64-bit
- Windows XP Embedded
- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows CE.NET 4.2 , 5.0 and 6.0
- MAC OS 8 / 9, OS-X
- Linux 2.4 and greater

.

Royalty-Free D2XX Direct Drivers (USB Drivers + DLL S/W Interface):

- Windows 7 32,64-bit
- Windows Vista
- Windows XP 64-bit
- Windows XP Embedded
- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows CE.NET 4.2, 5.0 and 6.0
- Linux 2.4 and greater

The drivers listed above are all available to download for free from www.ftdichip.com. Various 3rd Party Drivers are also available for other operating systems - visit www.ftdichip.com for details.

2.2 Features

The UM245R USB Parallel FIFO has the following features:

- Single chip USB to parallel FIFO bidirectional data transfer interface.
- Entire USB protocol handled on the chip – No USB-specific firmware programming required.
- Simple interface to MCU / PLD / FPGA logic with 4-wire handshake interface.
- Data transfer rate to 1 Megabyte / second - D2XX Direct Drivers.
- Data transfer rate to 300 kilobyte / second – VCP Drivers.
- FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- USB FTDIChip-ID™ feature.
- FIFO receive and transmit buffers for high data throughput.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR strobes allow the data bus to be used as a general purpose I/O port.
- Integrated 1024 bit internal EEPROM for storing USB VID, PID, serial number and product description strings.
- Device supplied pre-programmed with unique USB serial number.
- Support for USB suspend / resume through PWREN# pin and Wake Up pin function.
- In-built support for event characters.
- Support for bus powered, self powered, and high-power bus powered USB configurations.
- Integrated 3.3V level converter for USB I/O.
- Integrated level converter on FIFO interface and control pins for interfacing to 5V - 1.8V Logic.
- True 5V / 3.3V / 2.8V / 1.8V CMOS drive output and TTL input.
- High output drive option on I/O pins.
- Integrated USB termination resistors.
- Integrated power-on-reset circuit.
- Fully integrated clock - no external crystal, oscillator, or resonator required.
- Fully integrated AVCC supply filtering - No separate AVCC pin and no external R-C filter required.
- USB bulk transfer mode.
- 3.3V to 5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI / OHCI / EHCI host controller compatible
- USB 2.0 Full Speed compatible.
- -40°C to +85°C extended operating temperature range.
- Supplied in PCB designed to fit a standard 15.0mm (0.6") wide 24 pin DIP socket. Pins are on a 2.54mm (0.1") pitch.
- On board USB 'B' socket allows module to be connected to a PC via a standard A to B USB cable.

3 FT245RL Features and Enhancement

3.1 Key Features

This section summarises the key features and enhancements of the FT245R IC device which is used in the UM245R Module. For further details, consult the FT245R datasheet, which is available from the FTDI website.

Integrated Clock Circuit – Previous generations of FTDI's USB to parallel FIFO interface devices required an external crystal or ceramic resonator. The clock circuit has now been integrated onto the device meaning that no crystal or ceramic resonator is required. It is important to note that VCC must be between 4.0 and 5.25V. However, if required, an external 12MHz crystal can be used as the clock source.

Integrated EEPROM – Previous generations of FTDI's USB to parallel FIFO interface devices required an external EEPROM if the device were to use USB Vendor ID (VID), Product ID (PID), serial number and product description strings other than the default values in the device itself. This external EEPROM has now been integrated onto the FT245R chip meaning that all designs have the option to change the product description strings. A user area of the internal EEPROM is available for storing additional data. The internal EEPROM is programmable in circuit, over USB without any additional voltage requirement.

Pre-programmed EEPROM – The FT245R is supplied with its internal EEPROM pre-programmed with a serial number which is unique to each individual device. This, in most cases, will remove the need to program the device EEPROM.

Integrated USB Resistors – Previous generations of FTDI's USB to parallel FIFO interface devices required two external series termination resistors on the USBDP and USBDM signals, and a 1.5 kΩ pull up resistor on USBDP. These three resistors have now been integrated onto the device.

Integrated AVCC Filtering – Previous generations of FTDI's USB to parallel FIFO interface devices had a separate AVCC pin – the supply to the internal PLL. This pin required an external R-C filter. The separate AVCC pin is now connected internally to VCC, and the filter has now been integrated onto the chip.

Fewer External Components – Integration of the crystal, EEPROM, USB resistors, and AVCC filter will substantially reduce the bill of materials cost for USB interface designs using the FT245R compared to its FT245BM predecessor.

Enhanced Asynchronous Bit Bang Mode with RD# and WR# Strobes – The FT245R supports FTDI's BM chip bit bang mode. In bit bang mode, the eight parallel FIFO data bus lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT245R device this mode has been enhanced so that the internal RD# and WR strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the bit bang I/O bus. This option is described more fully in a application note AN232R-01, Bit Bang Modes for the FT232R and FT245R.

Synchronous Bit Bang Mode – Synchronous bit bang mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. The feature was previously seen in FTDI's FT2232D device. This option is described more fully in a application note AN232R-01, Bit Bang Modes for the FT232R and FT245R.

Lower Supply Voltage – Previous generations of the chip required 5V supply on the VCC pin. The FT245R will work with a VCC supply in the range 4.0V - 5V. Bus powered designs would still take their supply from the 5V on the USB bus. Self-powered designs must provide between 4.0V and 5.25V to VCC.

Integrated Level Converter on FIFO Interface and Control Signals – VCCIO pin supply can be from 1.8V to 5V. Connecting the VCCIO pin to 1.8V, 2.8V, or 3.3V allows the device to directly interface to 1.8V, 2.8V or 3.3V and other logic families without the need for external level converter ICs.

5V / 3.3V / 2.8V / 1.8V Logic Interface – The FT245R provides true CMOS Drive Outputs and TTL level Inputs.

Integrated Power-On-Reset (POR) Circuit – The device incorporates an internal POR function. A RESET# pin is available in order to allow external logic to reset the FT245R where required. With many applications the RESET# pin can be left unconnected, or pulled up to VCCIO.

Wake Up Function – If USB is in suspend mode and remote wake up has been enabled in the internal EEPROM (it is enabled by default), the RXF# pin becomes an input. Strobing this pin low will cause the FT245R to request a resume from suspend on the USB bus. Normally this can be used to wake up the host PC from suspend.

Lower Operating and Suspend Current – The device operating supply current has been further reduced to 15mA, and the suspend current has been reduced to around 70µA. This allows a greater margin for peripherals to meet the USB suspend current limit of 500µA (2.5mA with remote wake up enabled).

Low USB Bandwidth Consumption – The operation of the USB interface to the FT245R has been designed to use as little as possible of the total USB bandwidth available from the USB host controller.

High Output Drive Option – The parallel FIFO interface and the FIFO handshake output pins can be made to drive out at three times the standard signal drive level thus allowing multiple devices to be driven, or devices that require greater signal drive strength to be interfaced to the FT245R. This option is configured in the internal EEPROM.

Power Management Control for USB Bus Powered, High Current Designs – The PWREN# signal can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. An option in the internal EEPROM makes the device gently pull down on its FIFO interface lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

FTDIChip-ID™ - unique serial number which is burnt into the device at manufacture - This ID number cannot be reprogrammed by product manufacturers or end-users. This allows the possibility of using FT245R based dongles for software licensing. Further to this, a renewable license scheme can be implemented based on the FTDIChip-ID™ number when encrypted with other information. This encrypted number can be stored in the user area of the FT245R internal EEPROM, and can be decrypted, then compared with the protected FTDIChip-ID™ to verify that a license is valid. Web based applications can be used to maintain product licensing this way. An application note describing this feature is available separately from the FTDI website. The FTDIChip-ID is different from the USB Serial Number as defined in the USB specification.

Improved EMI Performance – The reduced operating current and improved on-chip VCC decoupling significantly improves the ease of PCB design requirements in order to meet FCC, CE and other EMI related specifications.

Programmable FIFO TX Buffer Timeout – The FIFO TX buffer timeout is used to flush remaining data from the receive buffer. This timeout defaults to 16ms, but is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be optimised for protocols that require fast response times from short data packets.

Extended Operating Temperature Range – The FT245R operates over an extended temperature range of -40º to +85º C thus allowing the device to be used in automotive and industrial applications.

New Package Options – The FT245R is available in two packages - a compact 28 pin SSOP (FT245RL) and an ultra-compact 5mm x 5mm pinless QFN-32 package (FT245RQ). Both packages are lead (Pb) free, and use a 'green' compound. Both packages are fully compliant with European Union directive 2002/95/EC.

4 UM245R Pin Out and Signal Descriptions

4.1 UM245R Pin Out

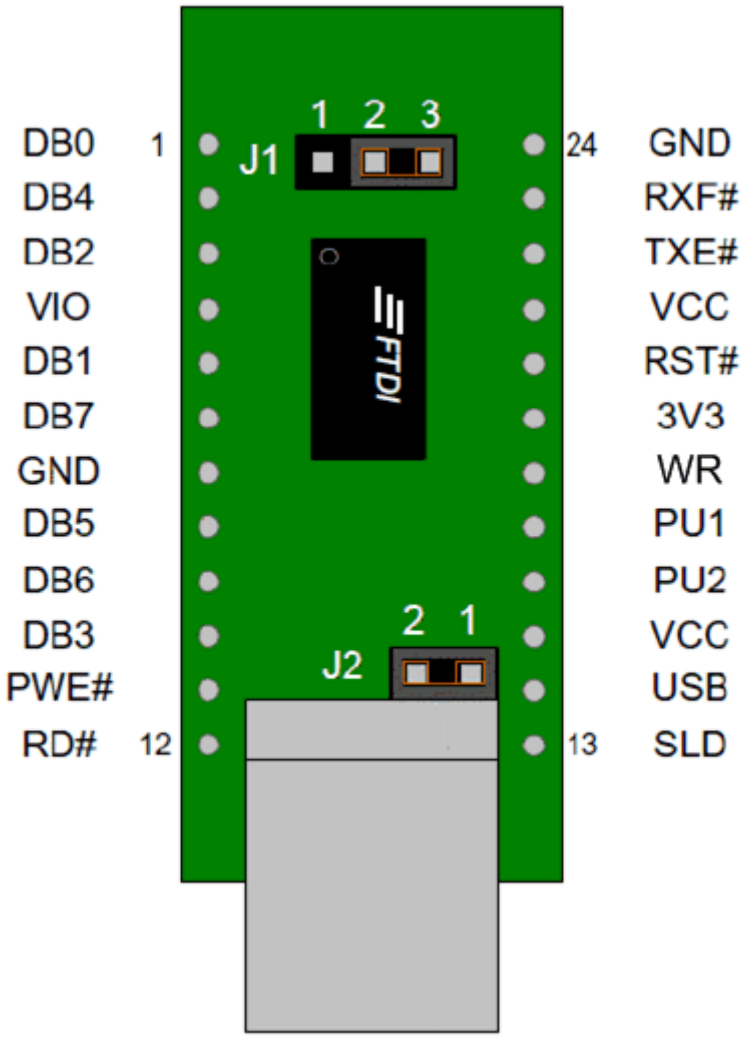

Figure 4.1 Module Pin Out and Jumper Locations

4.2 Signal Descriptions

Pin No.	Name	Type	Description
1	DB0	I/O	FIFO Data Bus Bit 0*
2	DB4	I/O	FIFO Data Bus Bit 4*
3	DB2	I/O	FIFO Data Bus Bit 2*
4	VIO	PWR	+1.8V to +5.25V supply to the FIFO Interface and Control group pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect to 3V3OUT to drive out at 3.3V levels (connect jumper J1 pins 1 and 2 together), or connect to VCC to drive at 5V CMOS level (connect jumper J1 pins 2 and 3 together). This pin can also be supplied with an external 1.8V – 5.0V supply in order to drive at different levels. It should be noted that in this case this supply should originate from the same source as the supply to Vcc. This means that in bus powered designs a regulator which is supplied by the 5V on the USB bus should be used.
5	DB1	I/O	FIFO Data Bus Bit 1*
6	DB7	I/O	FIFO Data Bus Bit 7*
7, 24	GND	PWR	Module ground supply pins
8	DB5	I/O	FIFO Data Bus Bit 5*
9	DB6	I/O	FIFO Data Bus Bit 6*
10	DB3	I/O	FIFO Data Bus Bit 3*
11	PWE#	I/O	Goes low after the device is configured by USB, then high during USB suspend. Can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# pin in this way.
12	RD#	I/O	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low. See Section 4.4 for timing diagram.*
13	SLD	GND	USB Cable shield.
14	USB	Output	5V Power output USB port. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design.
15, 21	VCC	PWR or Output	These two pins are internally connected on the module PCB. To power the module from the 5V supply on USB bus, connect jumper J2 pins 1 and 2 together (this is the module default configuration). In this case these pins would have the same description as pin 14. To use the UM245R module in a self powered configuration, ensure that jumper J2 pins 1 and 2 are not connected together, and apply an external 3.3V to 5.25V supply to one or both of these pins.
17	PU1	Control	Pull up resistor pin connection 2. Connect to pin 17 (RST#) in a self powered configuration.
16	PU2	Control	Pull up resistor pin connection 1. Connect to pin 14 (USB) in a self powered configuration.
19	3V3	Output	3.3V output from integrated LDO regulator. This pin is decoupled to ground on the module PCB with a 100nF capacitor. The prime purpose of this pin is to provide the internal 3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the FT245RL's VCCIO pin by connecting this pin to pin 4 (VIO), or by connecting together pins 1 and 2 on jumper J1.
20	RST#	Input	Can be used by an external device to reset the FT245R. If not required can be left unconnected, or pulled up to VCCIO.
18	WR	I/O	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low. See Section 4.4 for timing diagram.*

Pin No.	Name	Type	Description
22	TXE#	I/O	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 4.4 for timing diagram.
23	RXF#	I/O	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 4.4 for timing diagram. If the Remote Wakeup option is enabled in the internal EEPROM, during USB suspend mode (PWREN# = 1) RXF# becomes an input which can be used to wake up the USB host from suspend mode. Strobing the pin low will cause the device to request a resume on the USB bus.

Table 4.1 Module Pin-Out Description

* When used in Suspend, these pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal EEPROM.

4.3 Jumper Configuration Options

Pin No.	Name	Type	Description
1	3V3	Output	3.3V output from integrated LDO regulator. This pin is decoupled to ground on the module PCB with a 100nF capacitor. The prime purpose of this pin is to provide the internal 3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the FT245RL's VCCIO pin by connecting this pin to pin 4 (VIO), or by connecting together pins 1 and 2 on jumper J1.
2	VIO	PWR	+1.8V to +5.25V supply to the FIFO Interface and control pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect to 3V3 to drive out at 3.3V levels (connect jumper J1 pins 1 and 2 together), or connect to VCC to drive out at 5V CMOS level (connect jumper J1 pins 2 and 3 together). This pin can also be supplied with an external 1.8V - 2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to Vcc. This means that in bus powered designs a regulator which is supplied by the 5V on the USB bus should be used.
3	VCC	PWR	VCC Output. This will be 5V from the USB bus if pins 1 and 2 on jumper J2 are connected. Alternatively, if the module is in a self powered configuration, the supply to the VCC module pins (15 and 21) will be brought out to this jumper pin. Connect this jumper J1 pin 2 in order to supply the device IO pins from the supply to VCCIO.

Table 4.2 Jumper J1 Pin Description

Pin No.	Name	Type	Description
1	USB	PWR	5V Power output USB port. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design with the use of an external power switch (See Section 7.3).
2	VCC	PWR or Output	Board supply input. Connect to jumper J2 pin 1 in order to supply the board from the USB bus. This pin is internally connected to the VCC DIP pins. Remove the jumper connector in a self powered design.

Table 4.3 Jumper J2 Pin Description

4.4 FT245 FIFO Control Interface Read Cycle Timing Diagrams

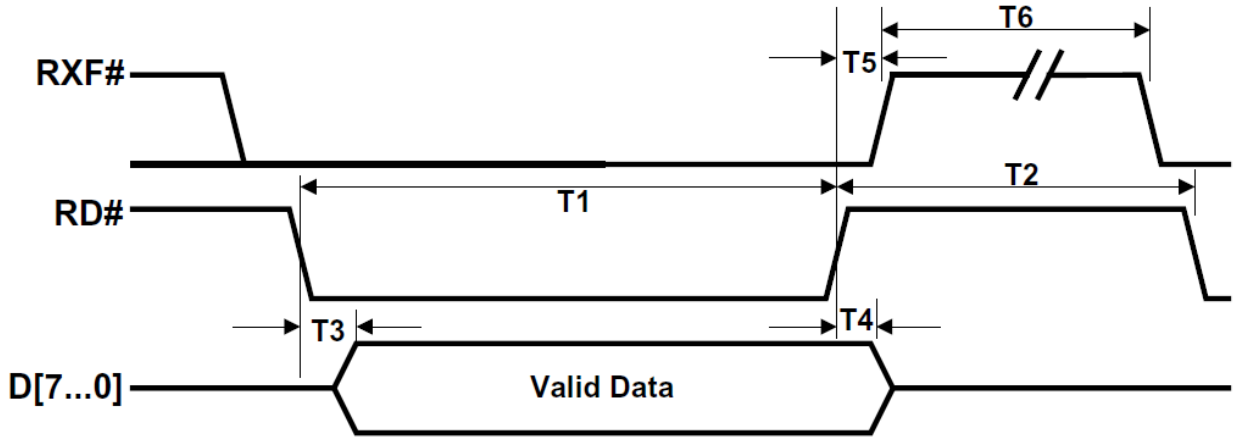

Figure 4.2 FIFO Read Cycle

Time	*Description*	*Min*	*Max*	*Unit*
T1	RD# Active Pulse Width	50		ns
T2	RD# to RD# Pre-Charge Time	50 + T6		ns
T3	RD# Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD# Inactive*	0		ns
T5	RD# Inactive to RXF#	0	25	ns
T6	RXF# Inactive After RD# Cycle	80		ns

Table 4.4 FIFO Read Cycle Timings

* Load = 30pF

4.5 FT245 FIFO Control Interface Write Cycle Timing Diagrams

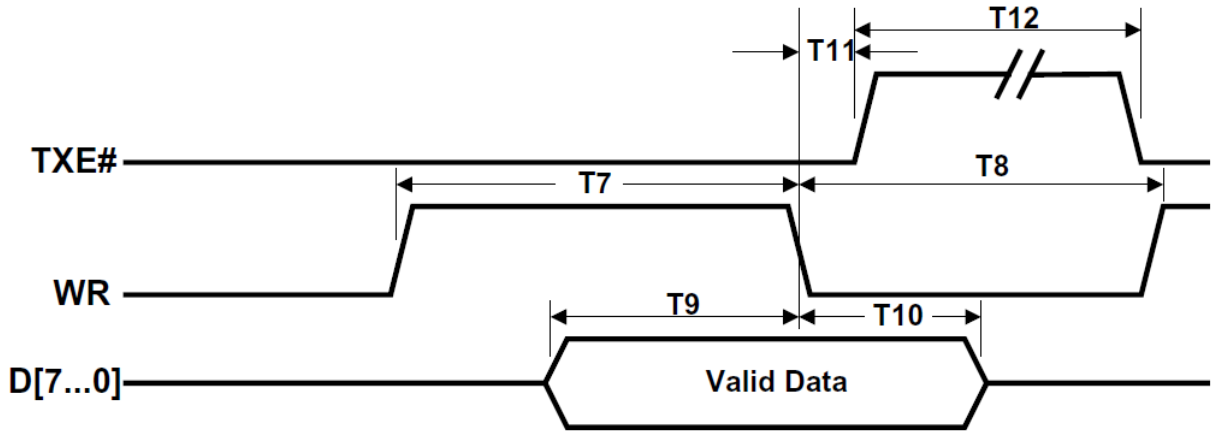

Figure 4.3 FIFO Write Cycle

Time	*Description*	*Min*	*Max*	*Unit*
T7	WR Active Pulse Width	50		ns
T8	WR to RD Pre-Charge Time	50		ns
T9	Data Setup Time before WR Inactive	20		ns
T10	Data Hold Time from RD Inactive	0		ns
T11	WR Inactive to TXE#	0	25	ns
T12	TXE# Inactive After WR Cycle	80		ns

Table 4.5 FIFO Write Cycle Timings

5 Module Dimensions

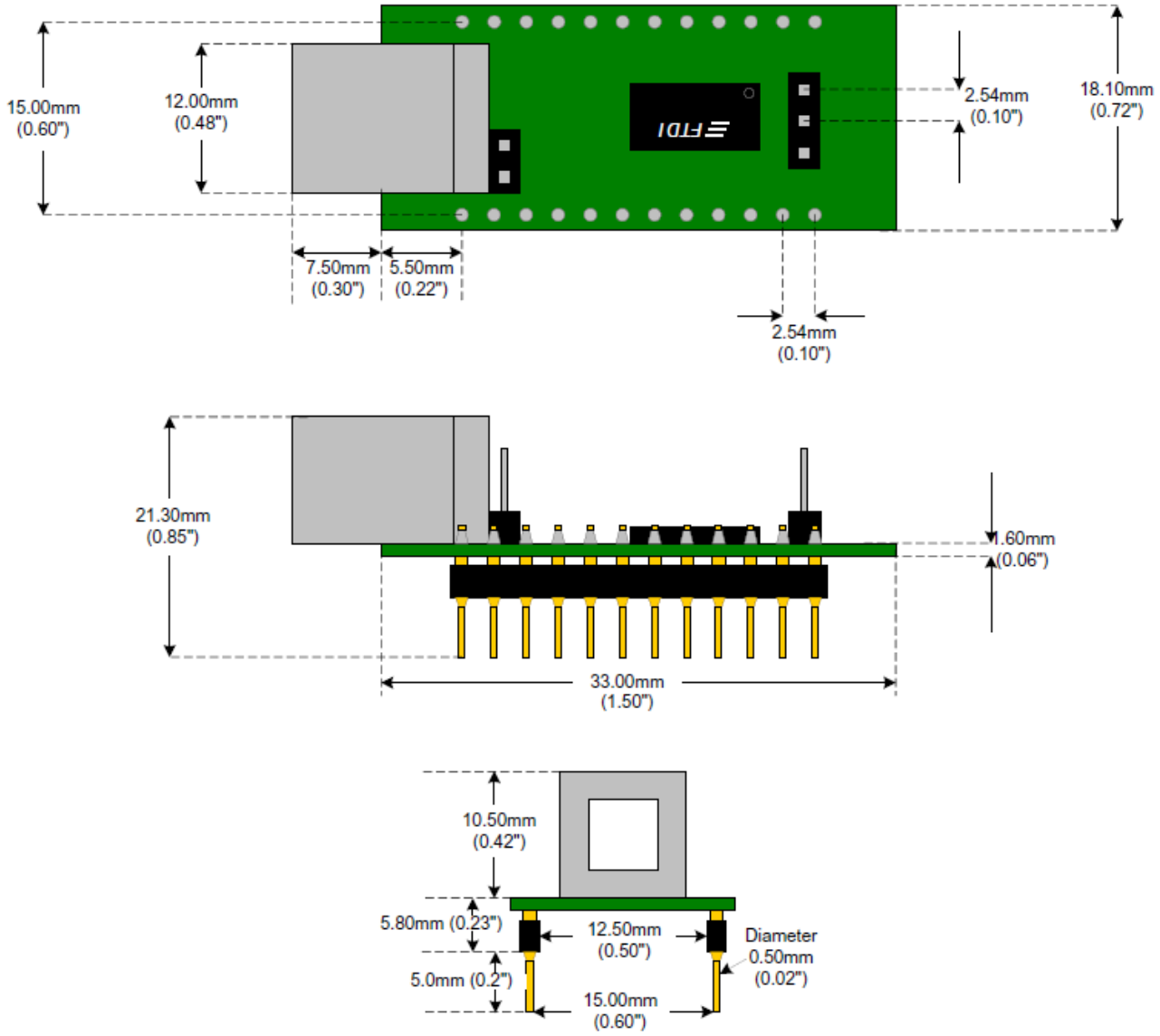

Figure 5.1 UM245R Module Dimensions

All dimensions are shown in millimeters with inches shown in parenthesis.
The FT245RL IC device used by the UM245R is supplied in a RoHS compliant 28 pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

The UM245R module uses exclusively lead free components.

Both the I.C. device and the module are fully compliant with European Union directive 2002/95/EC.

6 FT245RL Device Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT245R devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	*Value*	*Unit*
Storage Temperature	-65 to +150	°C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40 to +85	°C
VCC Supply Voltage	-0.5 to +6.00	V
D.C. Input Voltage - USBDP and USBDM	-0.5 to +3.8	V
D.C. Input Voltage - High Impedance Bidirectional signals	-0.5 to +(Vcc +0.5)	V
D.C. Input Voltage - All other Inputs	-0.5 to +(Vcc +0.5)	V
D.C. Output Current - Outputs	24	mA
DC Output Current - Low Impedance Bidirectionals	24	mA
Power Dissipation (Vcc = 5.25V)	500	mW

Table 6.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

6.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40 to 85°C)

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*	*Units*	*Conditions*
VCC1	VCC Operating Supply Voltage	4.0	---	5.25	V	The UM245R only uses the FT245R internal oscillator circuit
VCC2	VCCIO Operating Supply Voltage	1.8	---	5.25	V	
Icc1	Operating Supply Current	---	15	---	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	µA	USB Suspend

Table 6.2 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 6.3 FIFO Interface and Control Bus Pin Characteristics (VCCIO = 5.0V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 6.4 FIFO Interface and Control Bus Pin Characteristics (VCCIO = 3.3V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.6	3.1	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 6.5 FIFO Interface and Control Bus Pin Characteristics (VCCIO = 2.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 6.6 FIFO Interface and Control Bus Pin Characteristics (VCCIO = 5.0V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 6.7 FIFO Interface and Control Bus Pin Characteristics (VCCIO = 3.3V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 6.8 FIFO Interface and Control Bus Pin Characteristics (VCCIO = 2.8V, High Drive Level)

** Inputs have an internal 200kΩ pull-up resistor to VCCIO

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 6.9 RESET# and TEST Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8	---	3.6	V	RI = 1.5kΩ to 3V3Out (D+) RI = 15KΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0	---	0.3	V	RI = 1.5kΩ to 3V3Out (D+) RI = 15kΩ to GND (D-)
UVse	Single Ended Rx Threshold	0.8	---	2.0	V	
UCom	Differential Common Mode	0.8	---	2.5	V	
UVDif	Differential Input Sensitivity	0.2	---	---	V	
UDrvZ	Driver Output Impedance	26	29	44	Ohms	***

Table 6.10 USB I/O Pin (USBDP, USBDM) Characteristics

*** Driver Output Impedance includes the internal USB series resistors on USBDP and USBDM pins

6.3 EEPROM Reliability Characteristics

The internal 1024 bit EEPROM has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	15	Years
Read / Write Cycle	100,000	Cycles

Table 6.11 EEPROM Characteristics

6.4 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	*Value*			*Unit*
	Minimum	*Typical*	*Maximum*	
Frequency of Operation	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 6.12 Internal Clock Characteristics

NOTE: Use of the internal clock requires VCC to be in the range of 4.0V to 5.25V.

7 Module Configurations

7.1 BUS Powered Configuration

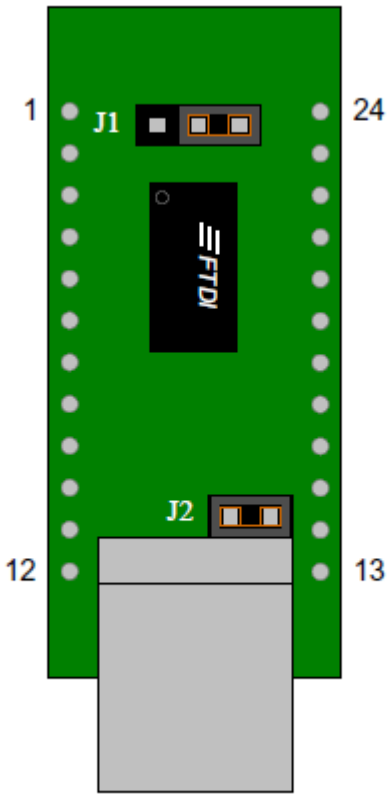

Figure 7.1 Bus Powered Configuration

Figure 7.1 illustrates the UM245R in a typical USB bus powered design configuration. This can easily be done by fitting the jumper link on J2, as shown above. The UM245R is supplied in this configuration by default. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows:

i) On plug-in to USB, the device must draw no more than 100mA.
ii) On USB Suspend the device must draw no more than 500µA (2.5mA if remote wake-up is enabled).
iii) A Bus Powered High Power USB Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500µA/2.5mA on USB suspend.
iv) A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub.
v) No device can draw more that 500mA from the USB Bus.

Interfacing the UM245R module to a microcontroller (MCU), or other logic for a bus powered design would be done in exactly the same way as for a self powered design (see Section 7.2), except that the MCU would take its power supply from the USB bus (either the 5V on the USB pin, or the 3.3V on the 3V3 pin).

7.2 Self Powered Configuration

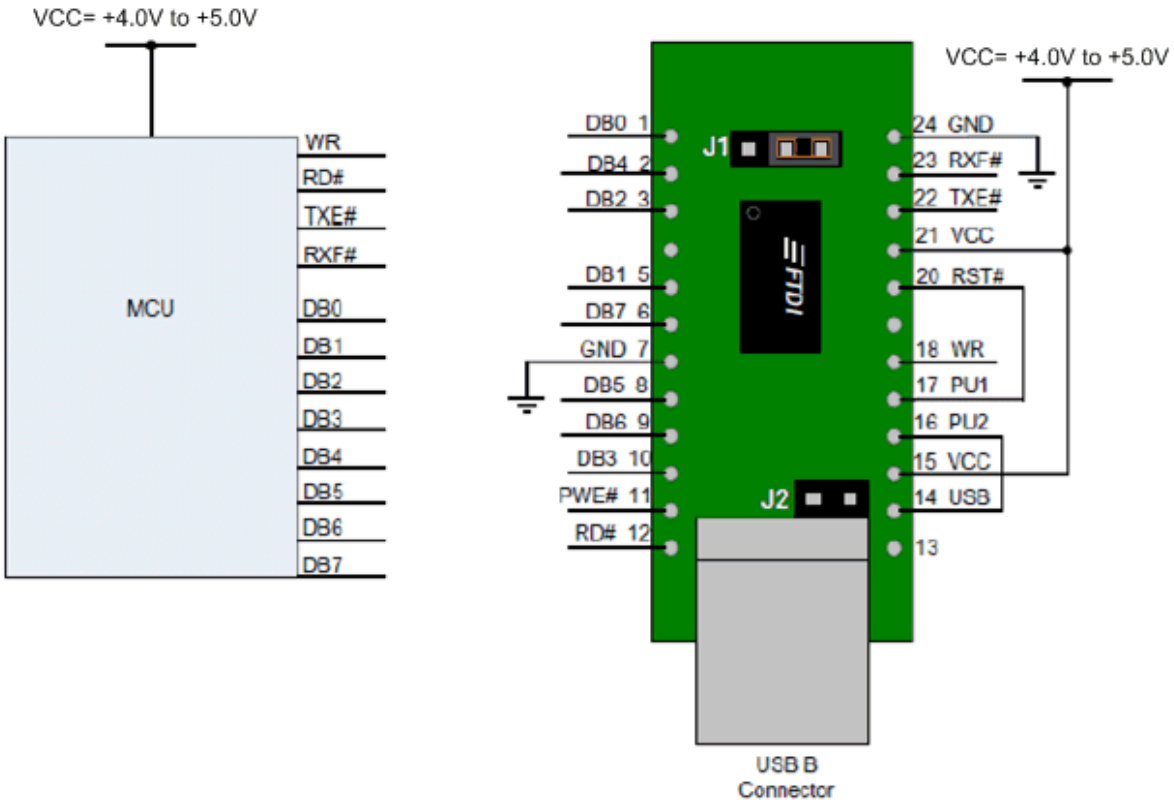

Figure 7.2 Self-Powered Configuration

Figure 7.2 illustrates the UM245R in a typical USB self powered configuration. In this case the link on jumper J2 is removed, and an external supply is connected to the module VCC pins. Figure 7.2 illustrate a design which has a 4.0V - 5V supply.

A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows:

i) A Self Powered device must not force current down the USB bus when the USB Host or Hub Controller is powered down.
ii) A Self Powered Device can use as much current as it likes during normal operation and USB suspend as it has its own power supply.
iii) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs

The power descriptor in the internal EEPROM should be programmed to a value of zero (self powered).

In order to meet requirement (i) the USB Bus Power is used to control the RESET# Pin of the FT245R device. When the USB Host or Hub is powered up the internal 1.5kΩ resistor on USBDP is pulled up to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, the internal 1.5kΩ resistor will not be pulled up to 3.3V, so no current will be forced down USBDP via the 1.5kΩ pull-up resistor when the host or hub is powered down. To do this pin 14 (USB) is connected to PU2 and PU1 is connected to RST#. Failure to do this may cause some USB host or hub controllers to power up erratically.

NOTE: When the FT245R is in reset, the FIFO interface and control pins all go tri-state. These pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

Figure 7.2 also illustrates interfacing the UM245R and a Microcontroller (MCU) FIFO interface. This example uses two MCU I/O ports: one port (8 bits) to transfer data, and the other port (4 or 5 bits) to monitor the TXE# and RXF# status bits and generate the RD# and WR strobes to the FT245R, as required. Using PWE# for this function is optional.

If the Remote Wakeup option is enabled in the internal EEPROM, during USB suspend mode RXF# becomes an input which can be used to wake up the USB host controller by strobing the pin low.

7.3 USB Bus Powered with Power Switching Confiduration

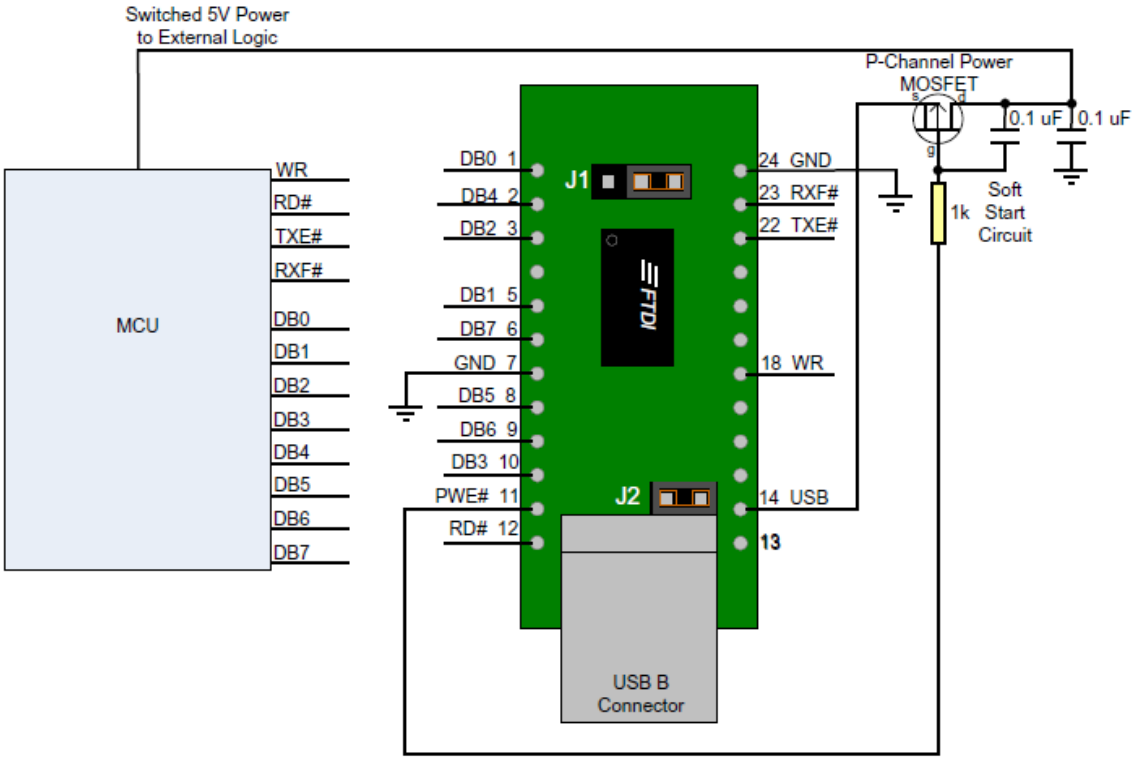

Figure 7.3 Bus Powered with Power Switching Configuration

USB Bus powered circuits need to be able to power down in USB suspend mode in order to meet the <= 500µA (2.5mA with remote wake-up enabled) total USB suspend current requirement, including external logic. Some external logic can power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT245R provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 7.3 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device would be an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1kΩ series resistor and a 0.1µF capacitor are used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT245R, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

Alternatively, a dedicated power switch I.C. with inbuilt "soft-start" can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (www.micrel.com) MIC2025-2BM or equivalent.

Please note the following points in connection with power controlled designs:

i) The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is re-applied on coming out of suspend.
ii) Set the Pull-down on Suspend option in the internal EEPROM.
iii) The PWE# pin should be used to switch the power to the external circuitry.
iv) For USB high-power bus powered device (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the device should be set in the max power field in the internal EEPROM. A high-power bus powered device must use this descriptor in the internal EEPROM to inform the system of its power requirements.
v) For 3.3V power controlled circuits the VCCIO pin must not be powered down with the external circuitry (the PWREN# signal gets its supply from VCCIO). Either connect the power switch between the output of the 3.3V regulator and the external 3.3V logic or power VCCIO from the 3V3OUT pin of the FT245R.

7.4 Bus Powered with 3.3V Logic Drive / IO Supply Voltage

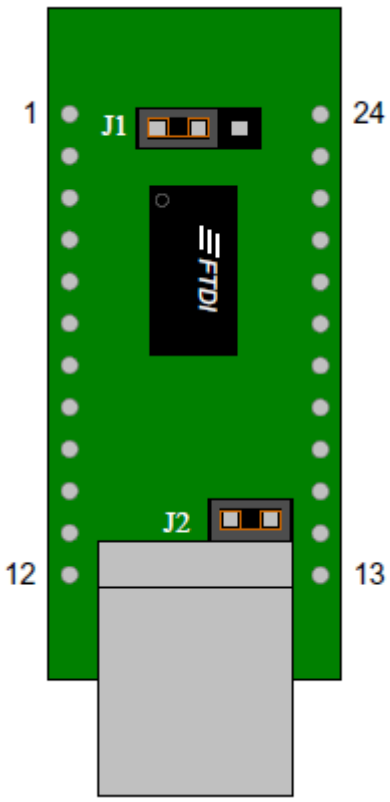

Figure 7.4 USB Bus Powered 3.3V Logic Drive

Figure 7.4 shows a configuration where a jumper switch is used to allow the FT245R to be interfaced with a 3.3V or 5V logic devices. The FT245R's VCCIO pin is either supplied with 5V from the USB bus (connect together pins 2 and 3 on J1), or with 3.3V from the FT245R's 3V3OUT pin (connect together pins 1 and 2 on J1 as shown). The supply to UM245R's 3V3 pin can also be used to supply up to 50mA to external logic.

Please note the following in relation to bus powered designs of this type:

i) The PWREN# signal should be used to power down external logic during USB suspend mode, in order to comply with the limit of 500µA (2.5mA with remote wake-up enabled). If this is not possible, use the configuration shown in Section 7.3

ii) The maximum current source from USB Bus during normal operation should not exceed 100mA, otherwise a bus powered design with power switching (Section 7.3) should be used.

Another possible configuration would be to use a discrete LDO which is supplied by the 5V on the USB bus to supply 2.8V - 1.8V to the VIO pin and to the external logic. VCC would be supplied with the 5V from the USB bus. With VIO connected to the output of the low dropout regulator would, in turn, will cause the FT245R I/O pins to drive out at 2.8V - 1.8V logic levels.

For USB bus powered circuits some considerations have to be taken into account when selecting the regulator:

iii) The regulator must be capable of sustaining its output voltage with an input voltage as low as 4.35V. A Low Drop Out (LDO) regulator must be selected.

iv) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500µA/2.5mA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip MCP17xx Series of devices (www.microchip.com). These devices can supply up to 250mA current and have a quiescent current of under 1µA.

8 UM245R Module Circuit Schematic

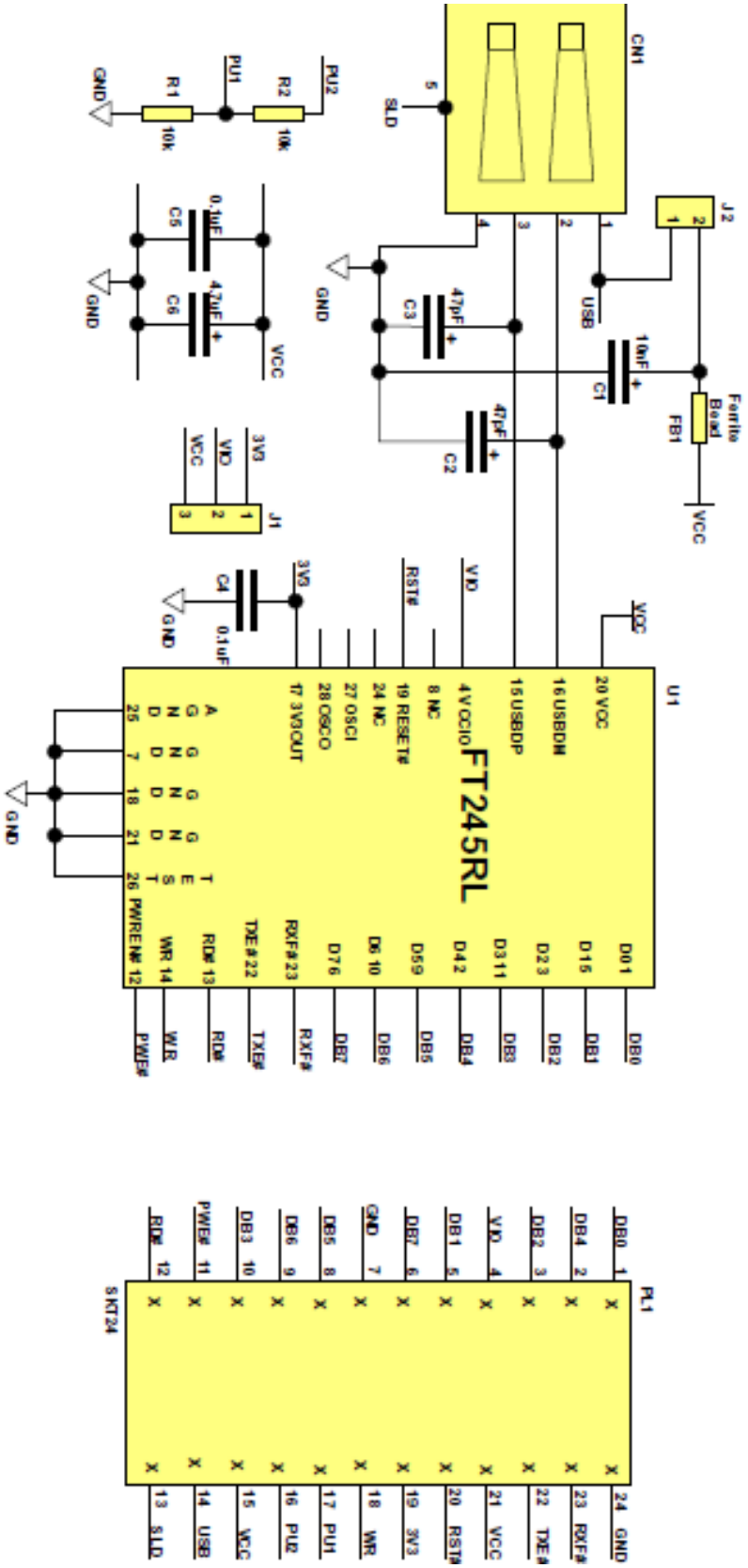

Figure 8.1 Module Circuit Schematic

9 Internal EEPROM Configuration

Following a power-on reset or a USB reset the FT245R will scan its internal EEPROM and read the USB configuration descriptors stored there. The default values programmed into the internal EEPROM in the FT245RL used on the UM245R are shown in Table 9.1.

Parameter	*Value*	*Notes*
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6001h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the EEPROM during final test of the UM245R module.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the FIFO interface lines when the power is shut off (PWREN# is high).
Manufacturer Name	FTDI	
Manufacturer ID	FT	Serial number prefix
Product Description	UM245R USB <-> Serial	
Max Bus Power Current	100mA	
Power Source	Bus Powered	
Device Type	FT245R	
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake Up	Enabled	Taking RI# low will wake up the USB host controller from suspend.
High Current I/Os	Disabled	Enables the high drive level on the FIFO data bus and control I/O pins.
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.

Table 9.1 Default Internal EEPROM Configuration

The internal EEPROM in the FT245R can be programmed over USB using the utility program FT_PROG. FT_PROG can be downloaded from the www.ftdichip.com. Users who do not have their own USB vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact FTDI Support (sales1@ftdichip.com) for this service.

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Appendix B – Revision History

Version 0.9	Initial Datasheet Created	December 2005
Version 1.00	Full Datasheet Release	December 2005
Version 1.01	Circuit Schematic Diagram Update	January 2006
Version 1.02	Module PCB Length Dimensions added	January 2006
Version 1.03	Table 4.1 (PU1 and PU2) Update	August 2009
	Contact information Update	August 2009
	Added Windows 7 32, 64 bit driver support	
Version 1.04	Added Document Reference No, FT_PROG	December 2009
	Corrected table 4.1- pin 5 DB5 changed to DB1	
	Updated formatting	
	Added 4.0V VCC/Internal Clock requirement	
	Corrected figures 4.1 and 7.2	