FAIRCHILD SEMICONDUCTOR™

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DM74LS161A/DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS161A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

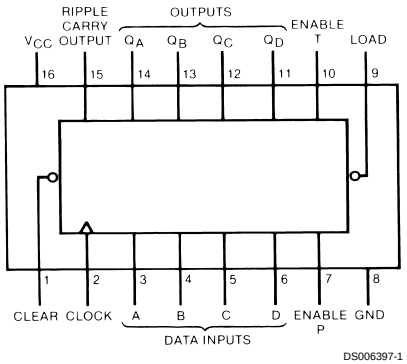
These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW

Connection Diagram

Dual-In-Line Package



Order Numbers 54LS161ADMQB, 54LS161AFMQB, 54LS161ALMQB, 54LS163ADMQB, 54LS163AFMQB, 54LS163ALMQB, DM54LS161AJ, DM54LS161AW, DM54LS163AJ, DM54LS163AW, DM74LS161AM, DM74LS161AN, DM74LS163AM or DM74LS163AN

See Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS161A			DM74LS161A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width	Clock	20	6		20	6		ns
	(Note 2)	Clear	20	9		20	9		
	Pulse Width	Clock	25			25			ns
	(Note 3)	Clear	25			25			
t_{SU}	Setup Time	Data	20	8		20	8		ns
	(Note 2)	Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time	Data	20			20			ns
	(Note 3)	Enable P	30			30			
		Load	30			30			
t_H	Hold Time	Data	0	−3		0	−3		ns
	(Note 2)	Others	0	−3		0	−3		
	Hold Time	Data	5			5			ns
	(Note 3)	Others	5			5			
t_{REL}	Clear Release Time (Note 2)		20			20			ns
	Clear Release Time (Note 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5.5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5.5V.

'LS161 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

’LS161 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	µA
			Clock			40	
			Load			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 6)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 7)			19	32	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 7: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

’LS161 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		28		45	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS163A			DM74LS163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 8)		0		25	0		25	MHz
	Clock Frequency (Note 9)		0		20	0		20	MHz
t_W	Pulse Width	Clock	20	6		20	6		ns
	(Note 8)	Clear	20	9		20	9		
	Pulse Width	Clock	25			25			ns
	(Note 9)	Clear	25			25			
t_{SU}	Setup Time	Data	20	8		20	8		ns
	(Note 8)	Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time	Data	20			20			ns
	(Note 9)	Enable P	30			30			
		Load	30			30			
t_H	Hold Time	Data	0	−3		0	−3		ns
	(Note 8)	Others	0	−3		0	−3		
	Hold Time	Data	5			5			ns
	(Note 9)	Others	5			5			
t_{REL}	Clear Release Time (Note 8)		20			20			ns
	Clear Release Time (Note 9)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 8: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 9: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

'LS163 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 10)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max	Enable T			0.2	mA
	Input Voltage	V_I = 7V	Clock, Clear			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input	V_{CC} = Max	Enable T			40	µA
	Current	V_I = 2.7V	Load			40	
			Clock, Clear			40	
			Others			20	

’LS163 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 10)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock, Clear			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 11)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 12)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 13)			18	32	mA

Note 10: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 11: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 12: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 13: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

’LS163 Switching Characteristics

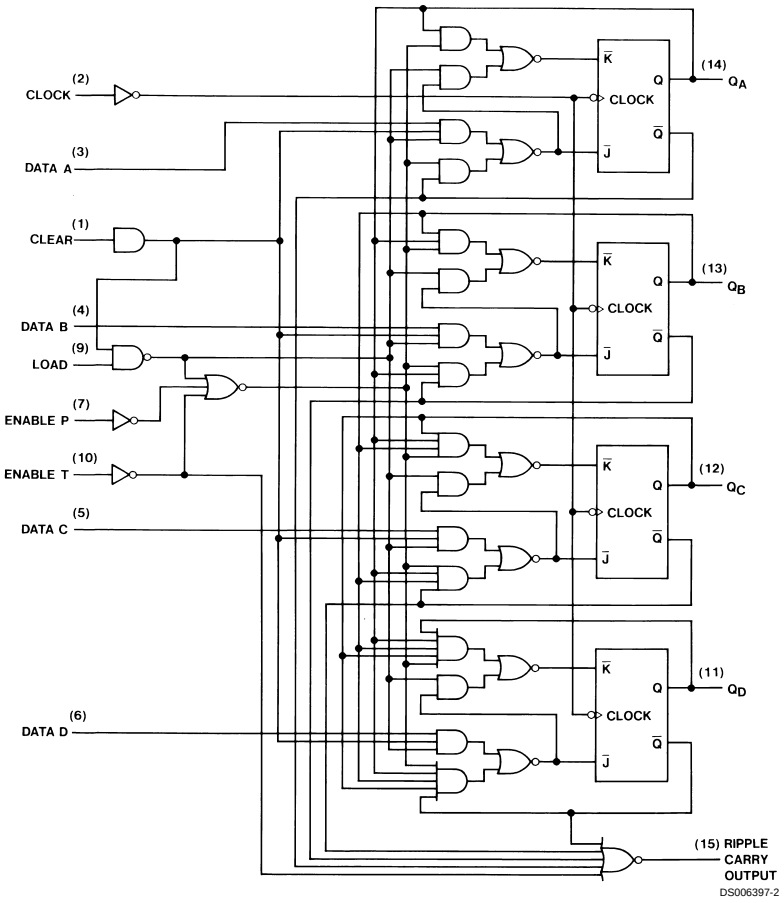
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q (Note 14)		28		45	ns

Note 14: The propagation delay clear to output is measured from the clock input transition.

Logic Diagram

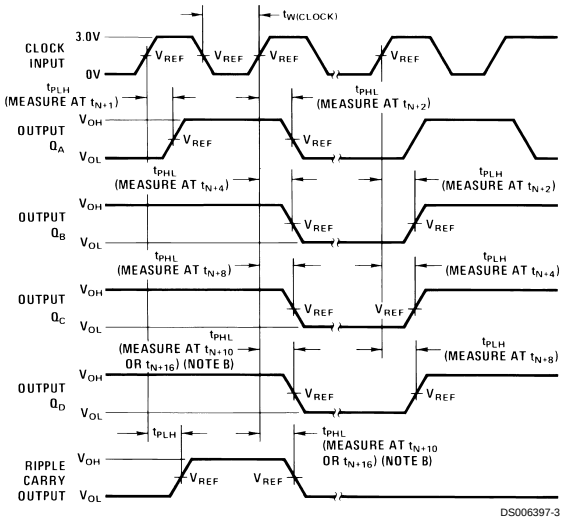
LS163A



The LS161A is similar, however, the clear buffer is connected directly to the flip flops.

Parameter Measurement Information

Switching Time Waveforms



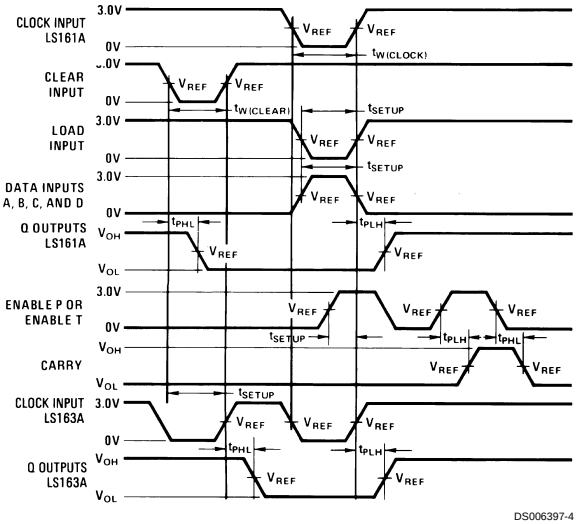
DS006397-3

Note 15: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note 16: Outputs Q_D and carry are tested at t_{n+16} where t_n is the bit time when all outputs are low.

Note 17: $V_{REF} = 1.5V$.

Switching Time Waveforms



DS006397-4

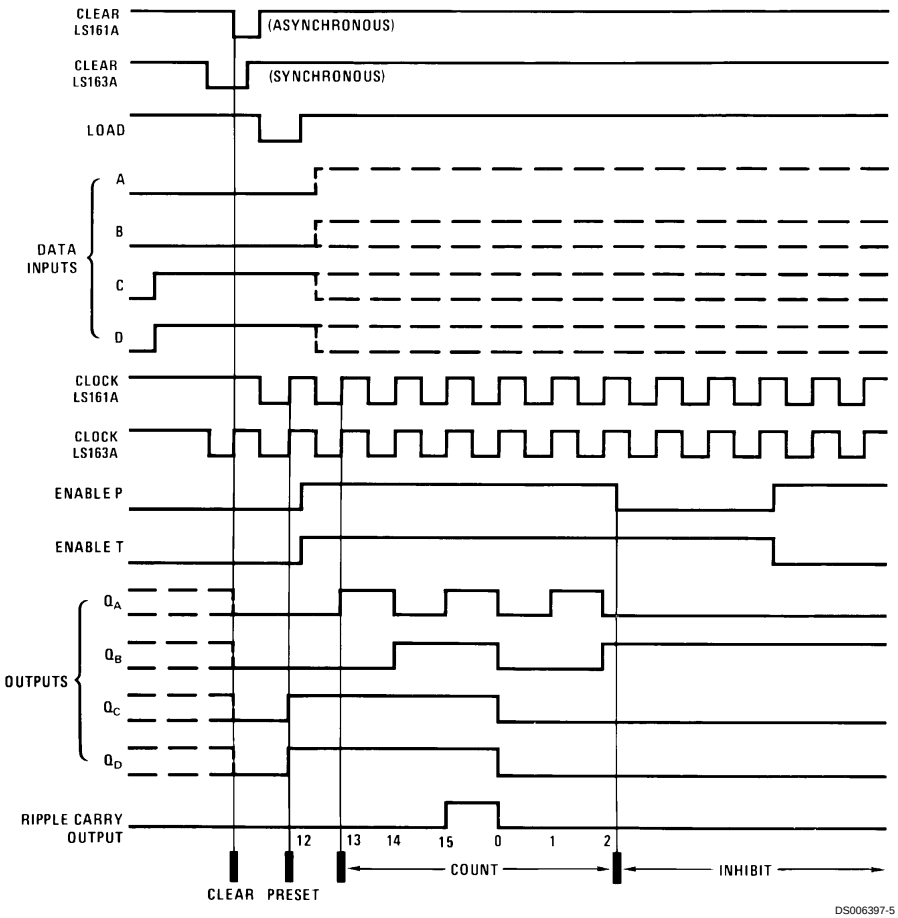
Note 18: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX}.

Note 19: Enable P and enable T setup times are measured at t_{n+0}.

Note 20: $V_{REF} = 1.3V$.

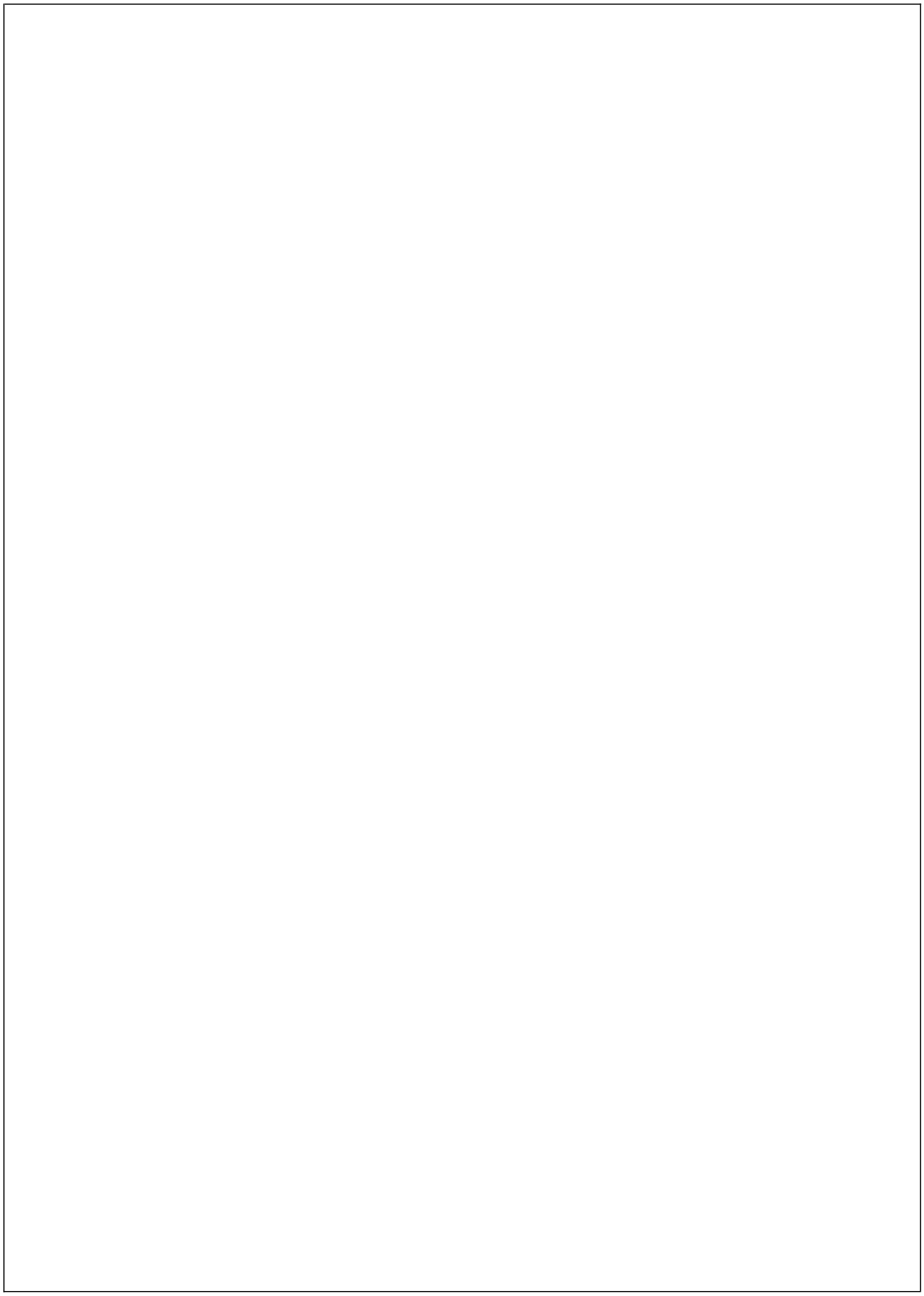
Timing Diagram

LS161A, LS163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences

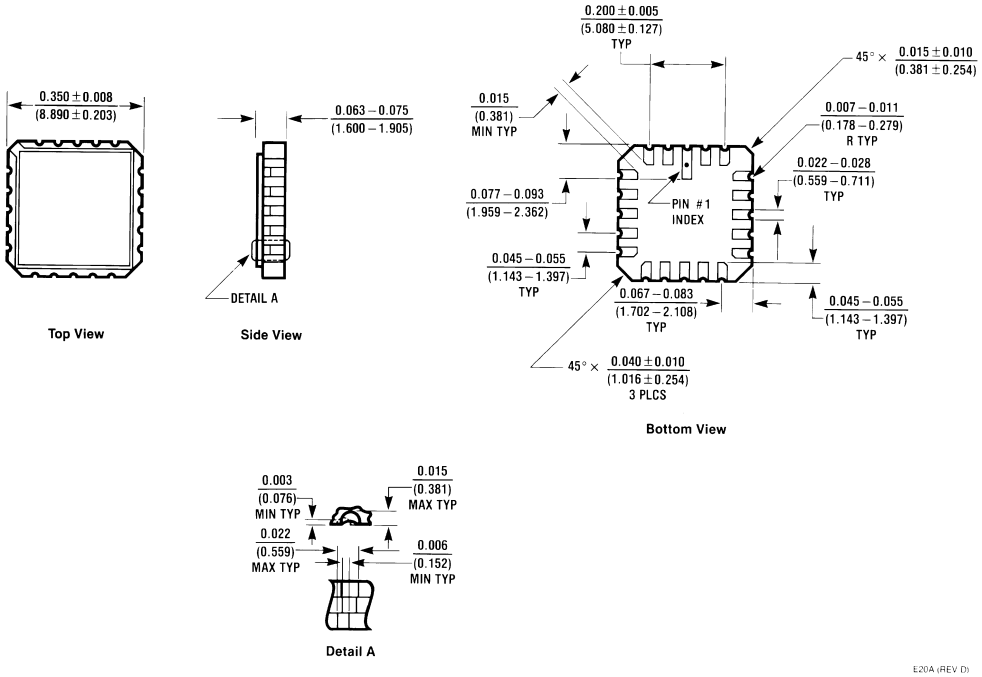


Sequence:

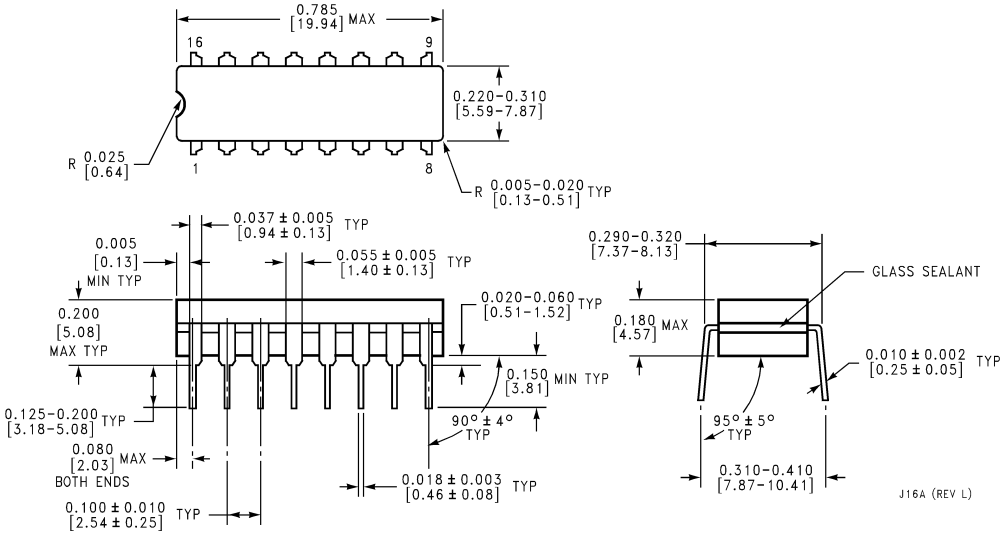
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit



Physical Dimensions inches (millimeters) unless otherwise noted

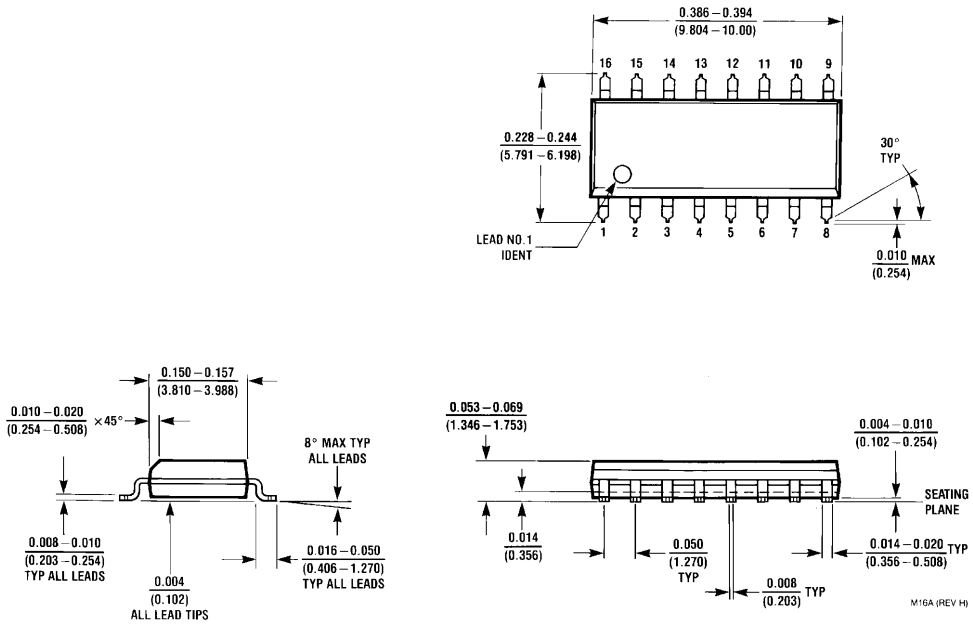


Ceramic Leadless Chip Carrier Package (E)
Order Numbers 54LS161ALMQB or 54LS163ALMQB
Package Number E20A

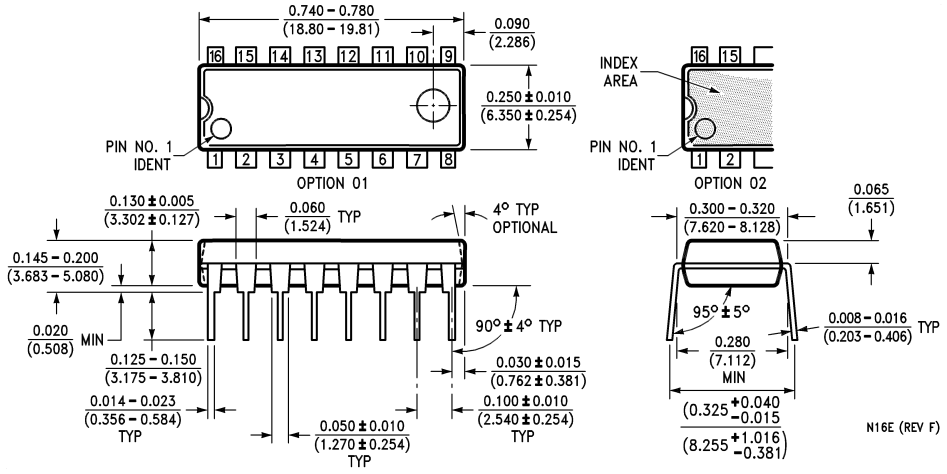


16-Lead Ceramic Dual-In-Line Package (J)
Order Numbers 54LS161ADMQB, 54LS163ADMQB, DM54LS161AJ or DM54LS163AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

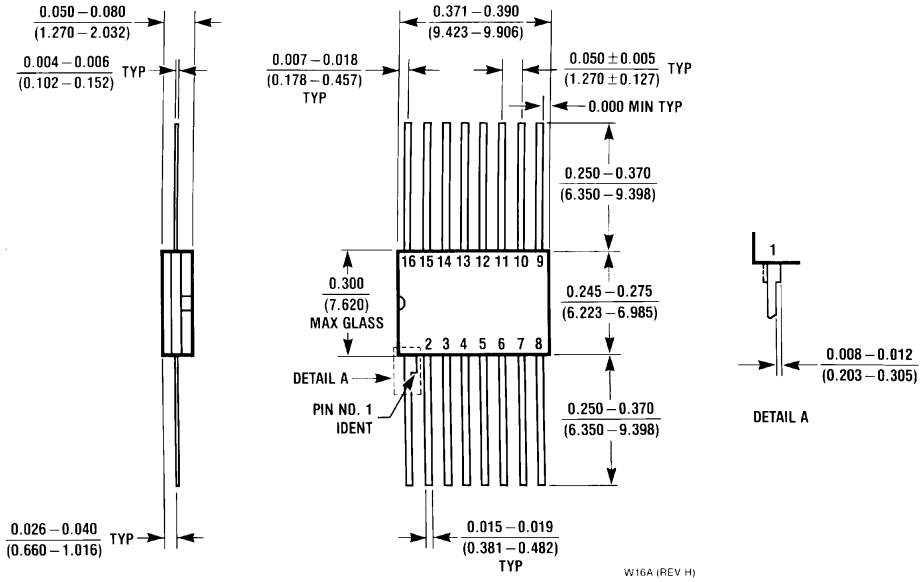


16-Lead Small Outline Molded Package (M)
Order Number DM74LS161AM or DM74LS163AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Numbers DM74LS161AN, DM74LS163AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Numbers 54LS161AFMQB, 54LS163AFMQB, DM54LS161AN or DM54LS163AW
Package Number W16A

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